XA-9485A
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Masaya MURANAKA et al.

Appln. No.:

Filed: HEREWITH

For: METHOD OF DECIDING ERROR RATE AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination, please amend the above-identified patent application as indicated below.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks begin on page 5 of this paper.